

FIG. 1

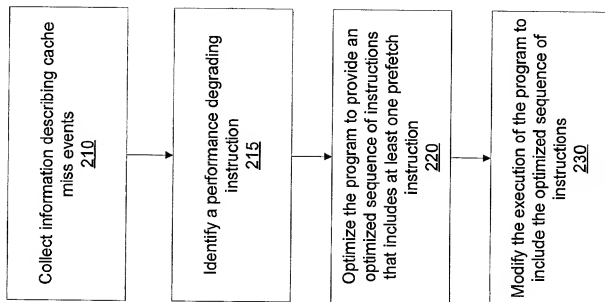


FIG. 2

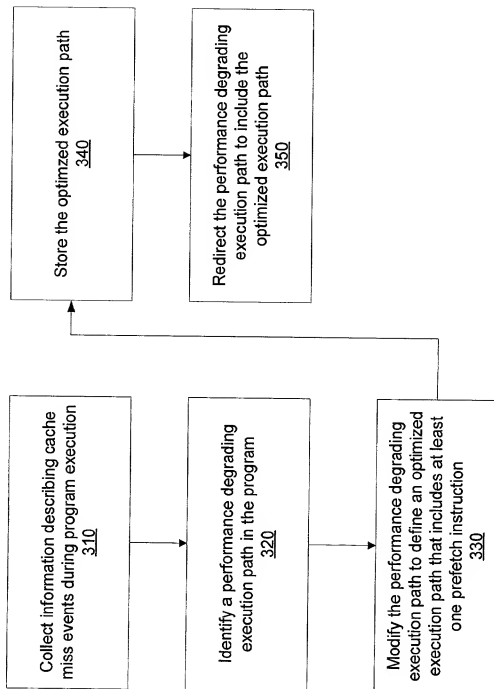


FIG. 3

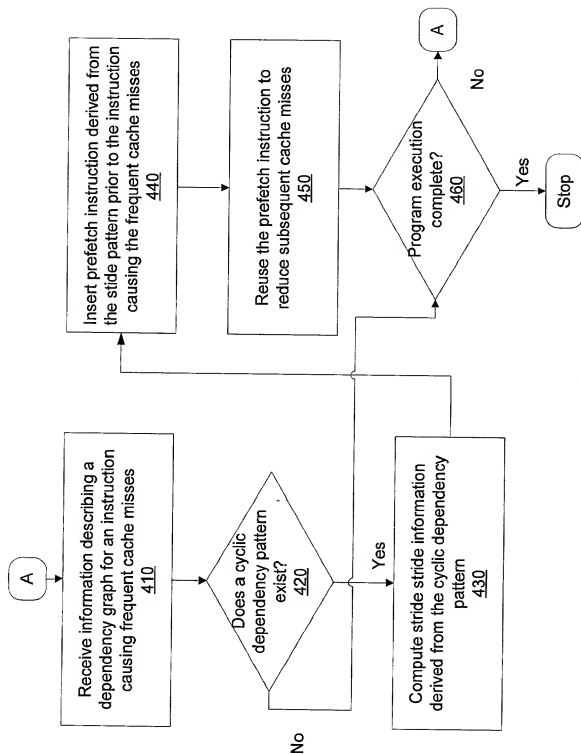
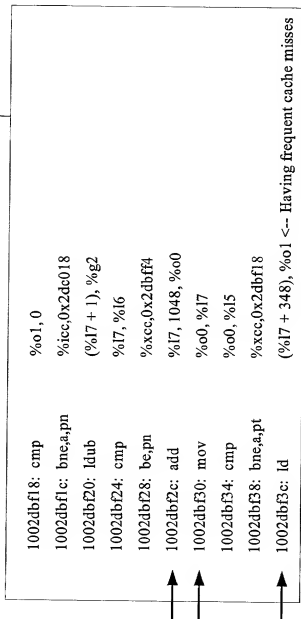


FIG. 4

510



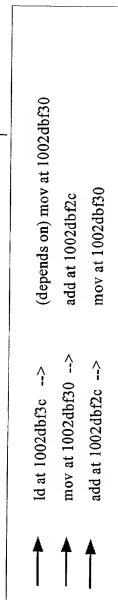
Add 550

Move 540

Load 520

FIG. 5A

530



Load 520

Move 540

Add 550

FIG. 5B

1002dbf18: cmp %o1, 0
1002dbf1c: bnc,a,pn %acc,0x2dc018
1002dbf20: ldub (%i7 + 1), %g2
1002dbf24: cmp %i7, %i6
1002dbf28: be,pn %xccc,0x2dbff4
1002dbf2c: add %i7, 1048, %i7
1002dbf30: ldix (%i7), %o1
1002dbf34: cmp %o0, %i5
1002dbf38: bne,a,pt %xccc,0x2dbf18
1002dbf3c: ld (%o1 + 348), %o1 <--- Having frequent cache misses

FIG. 5C

ld at 1002dbf3c --> ldix at 1002dbf30
ldix at 1002dbf30 --> add at 1002dbf2c
add at 1002dbf2c --> add at 1002dbf2c

FIG. 5D

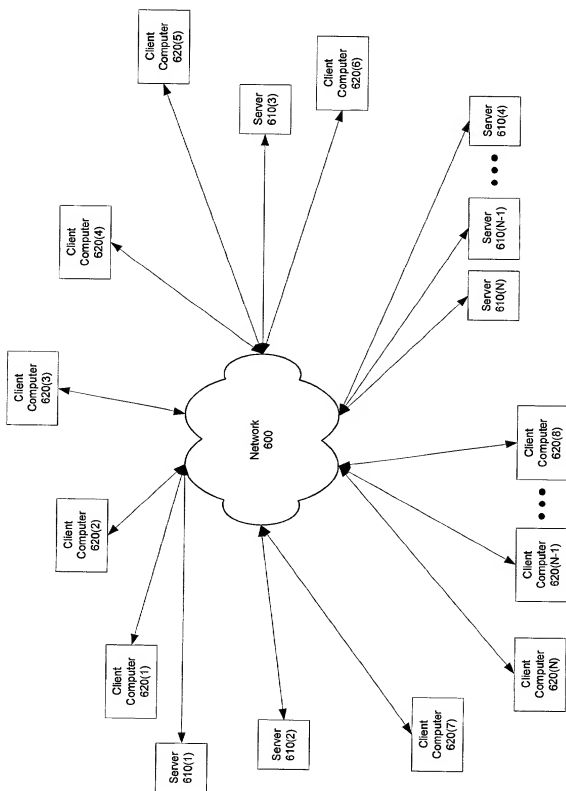


FIG. 6

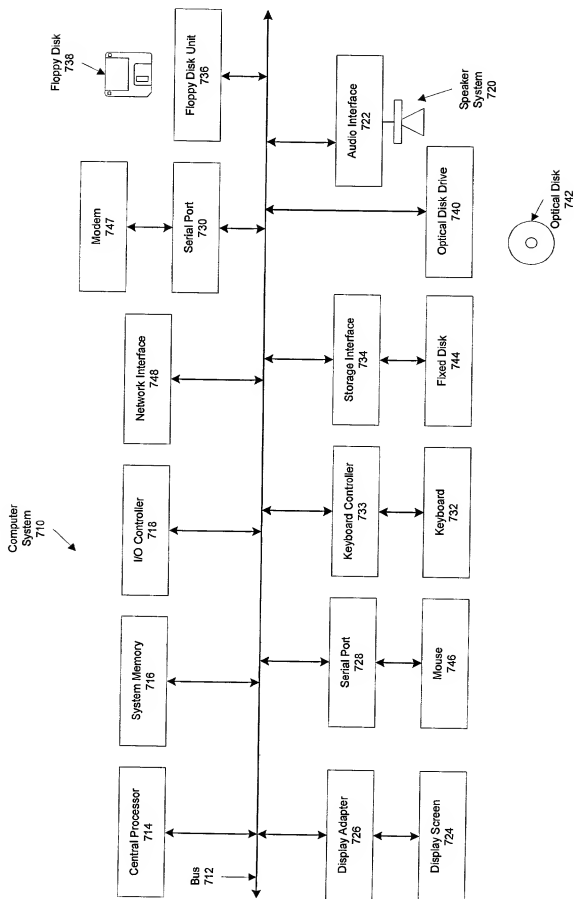


FIG. 7

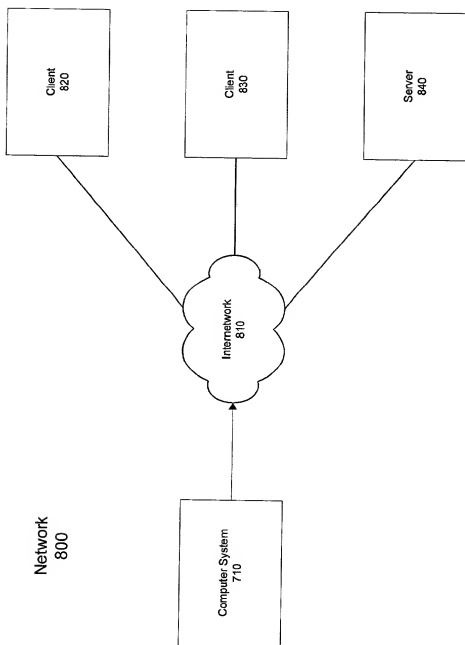


FIG. 8